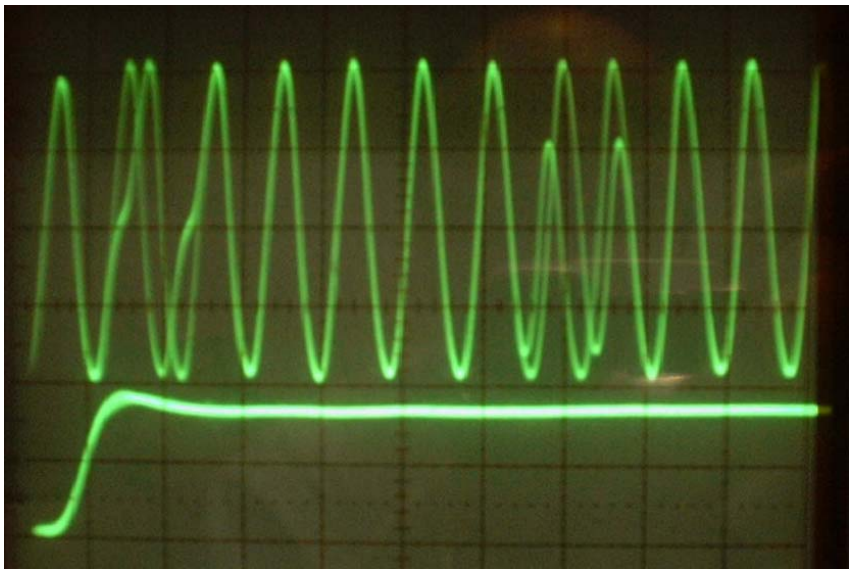
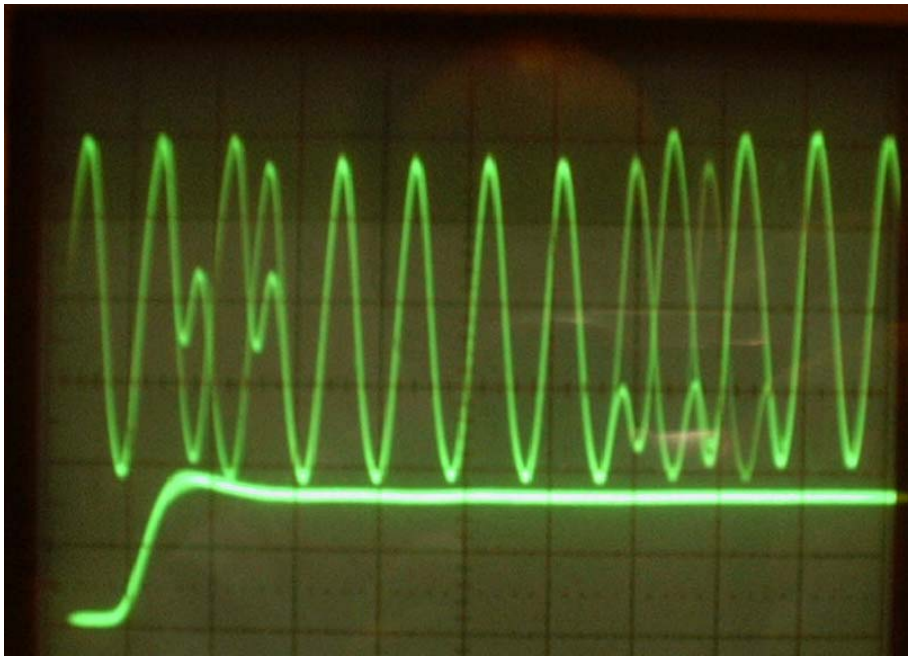
Data Patterns and Rates as Recovered (6/2/03)

Descriptive information regarding MSB modulation and detection is at the end.

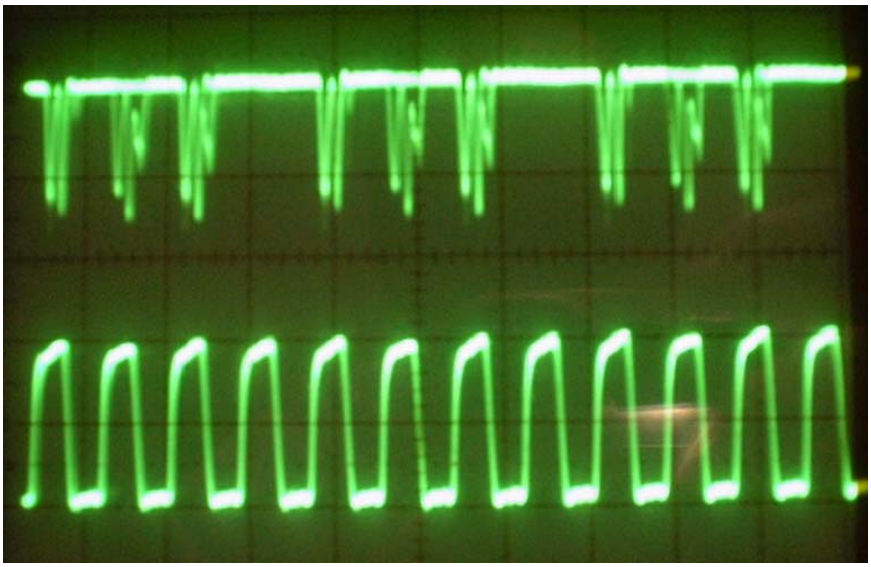


3PSK -------7 altered cycles. This method uses a 90 degree phase shift for a limited number of cycles.

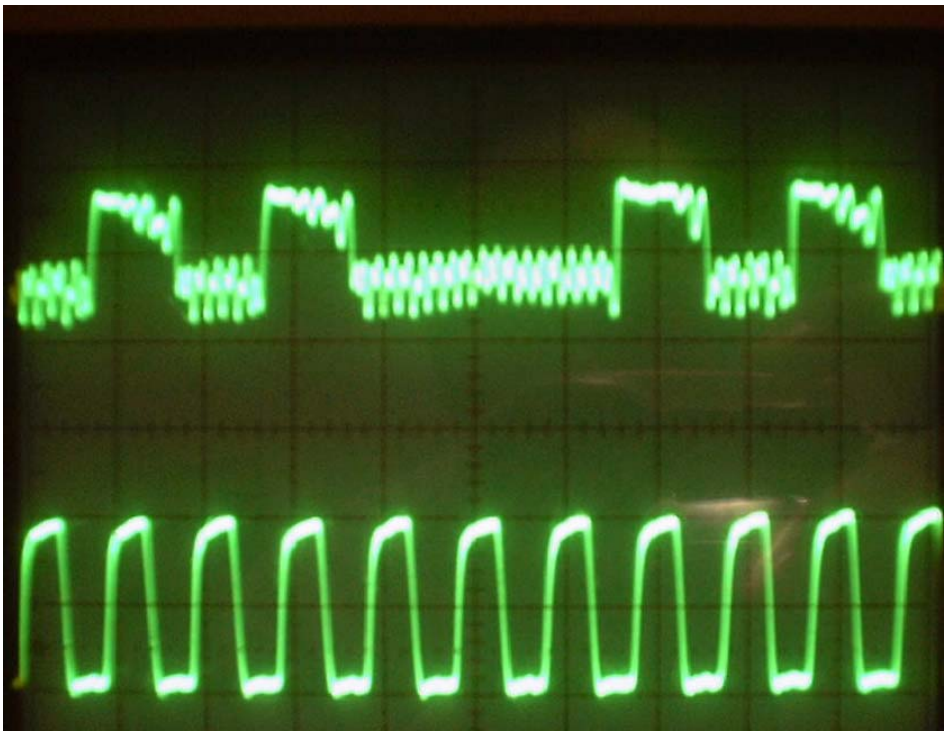


3PRK --7 altered cycles.. The method uses "pulse position phase reversal keying" (3PRK) (180 degree shift) for a limited number of cycles. Usually only one or two.

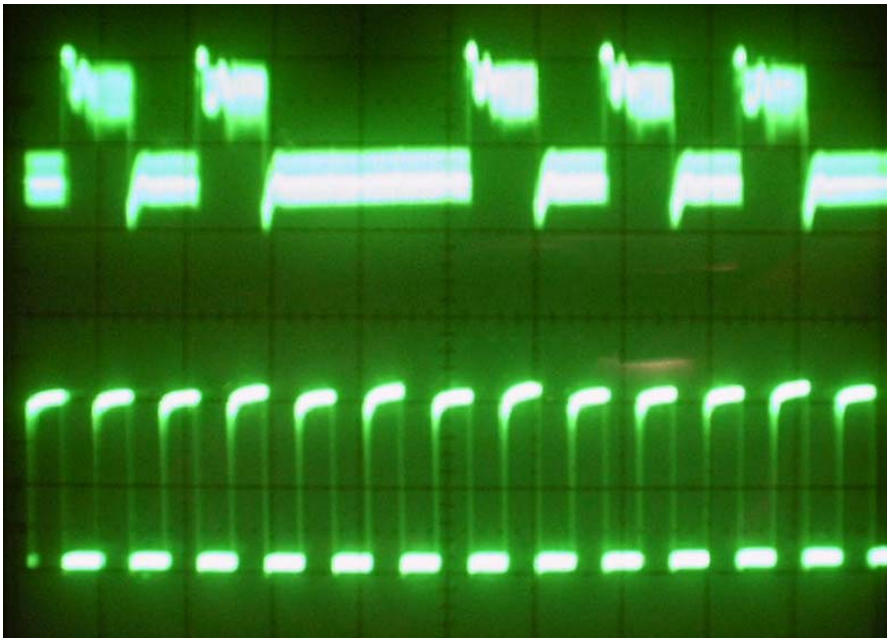
The following photos are for a discrete component phase detector that can resolve 1 RF cycle. 74AC components are used. (74AC86).



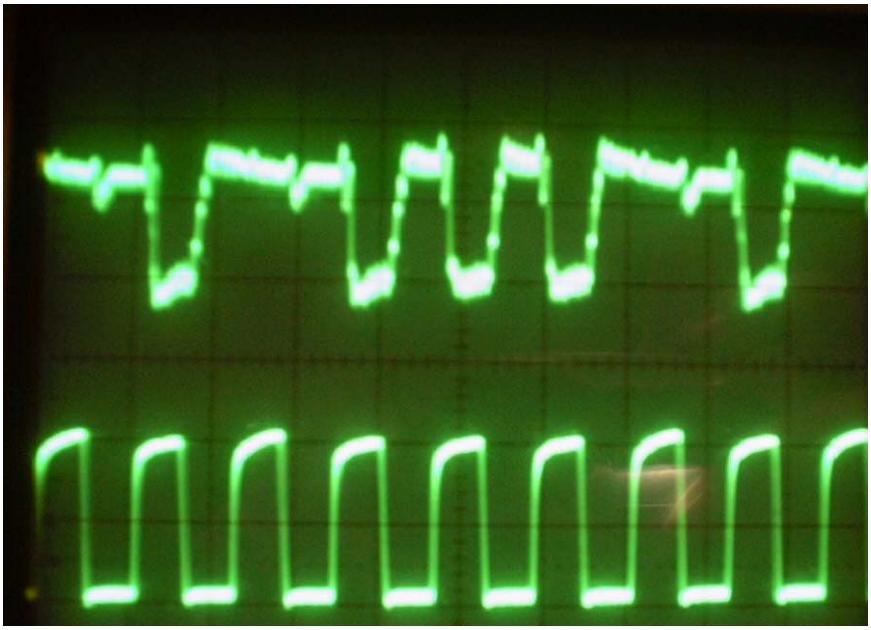
WPSK at 4 Mb/s Equivalent to 8 Mb/s NRZ. There are 3 RF cycles per phase change. 6 cycles out of the 24 Mb/s rate are used per bit. Only the leading cycle change is used. This sets a pulse stretcher, which presents a steady pulse for the data sampler. The leading edge of the RZ encoded data and the IF frequency are sycnchronized. The IF frequency is 24 Mhz. The phase detector can resolve one RF cycle.



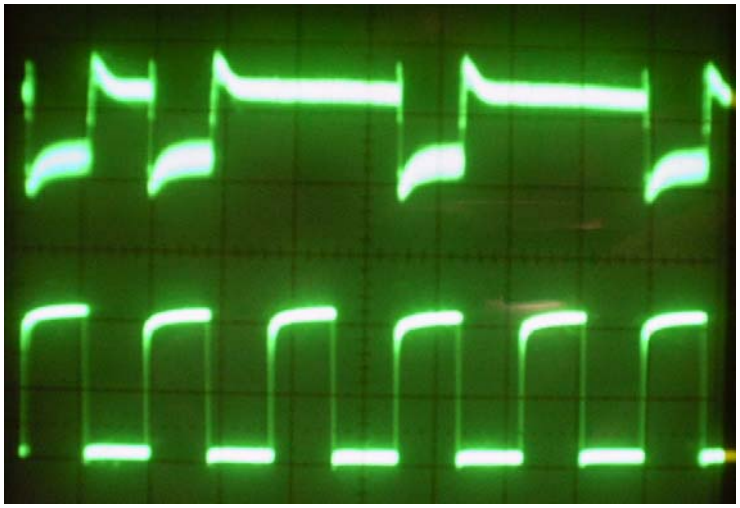
4 Mb/s NRZ 6 cycles per bit, one or zero. 24 MHz IF. Data Clock is lower trace.
20 MHz scope bandpass.



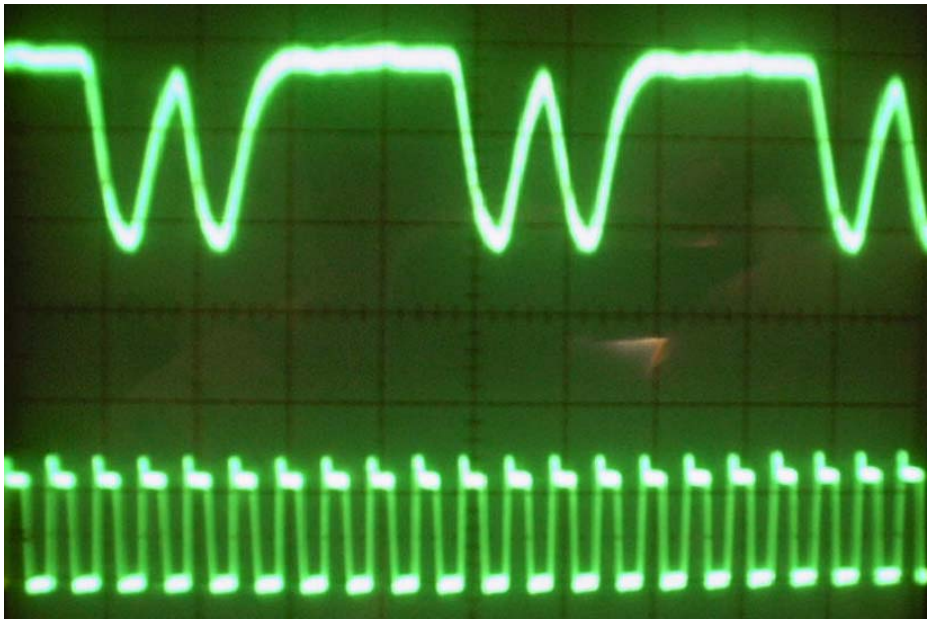
1.7 Mb/s NRZ input. The larger number of IF cycles per bit is becoming apparent.



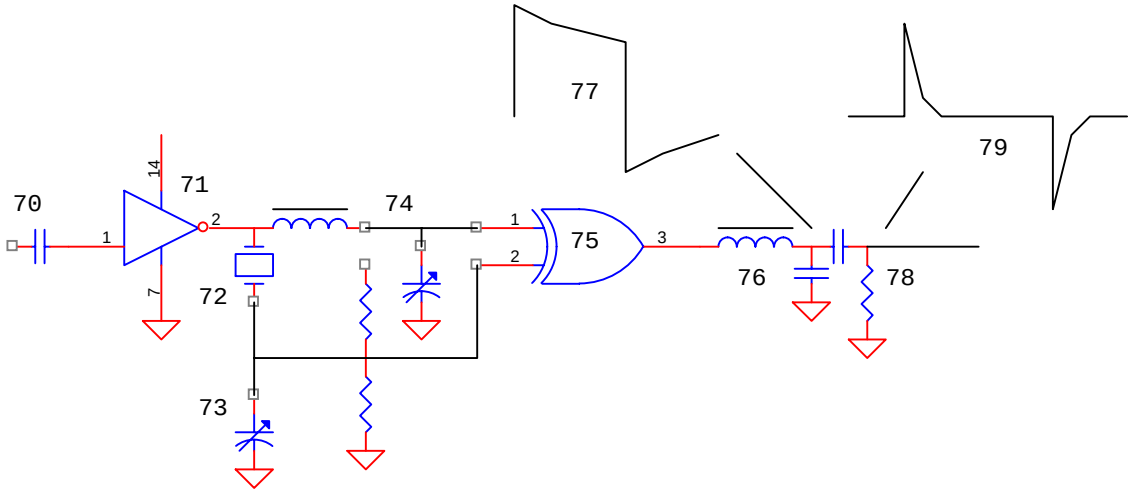
1.7 WPSK. RZ baseband encoding and 90 degree phase shift with approximately 7 cycles per shift period. This is equivalent to 3.4 Mb/s NRZ coding. The data rate can be increased using NRZ encoding, but there is more DC creep with NRZ coding.



270 kb/s WPSK. At this low data rate there are approximately 45 cycles per phase change. Increasing the rate to 812.5 kb/s for GSM EDGE equivalent is no problem, since that is double the number of cycles seen for 1.7 Mb/s WPSK above.



4 Mb/s NRZ Using SA636 Detector. Voltage slicing will restore the NRZ data pattern. The SA636 has an Op. Amp. following a Gilbert Cell phase detector. This creates a rise time problem (slew rate). 2-3 IF cycles are required to obtain near full phase detector output. The output voltage level is low and must be further amplified to be useful.



Discrete component phase detector used for the above photos. The amplifier 71 is a limiter to bring the input signal up to CMOS levels. The crystal 72 is used in a series mode to provide a phase reference (similar to a quadrature coil). The XOR gate 75 is a linear phase detector with rail to rail output for 180 degrees of phase shift. The vertical oscilloscope scale in the above photos is 2 volts per division, except for the SA 636 photo, which is amplified after the 636 op. Amp.

In some cases, it is advisable to differentiate the signal before decoding.

Properly designed and tuned zero group delay filters have very little phase shift loss.