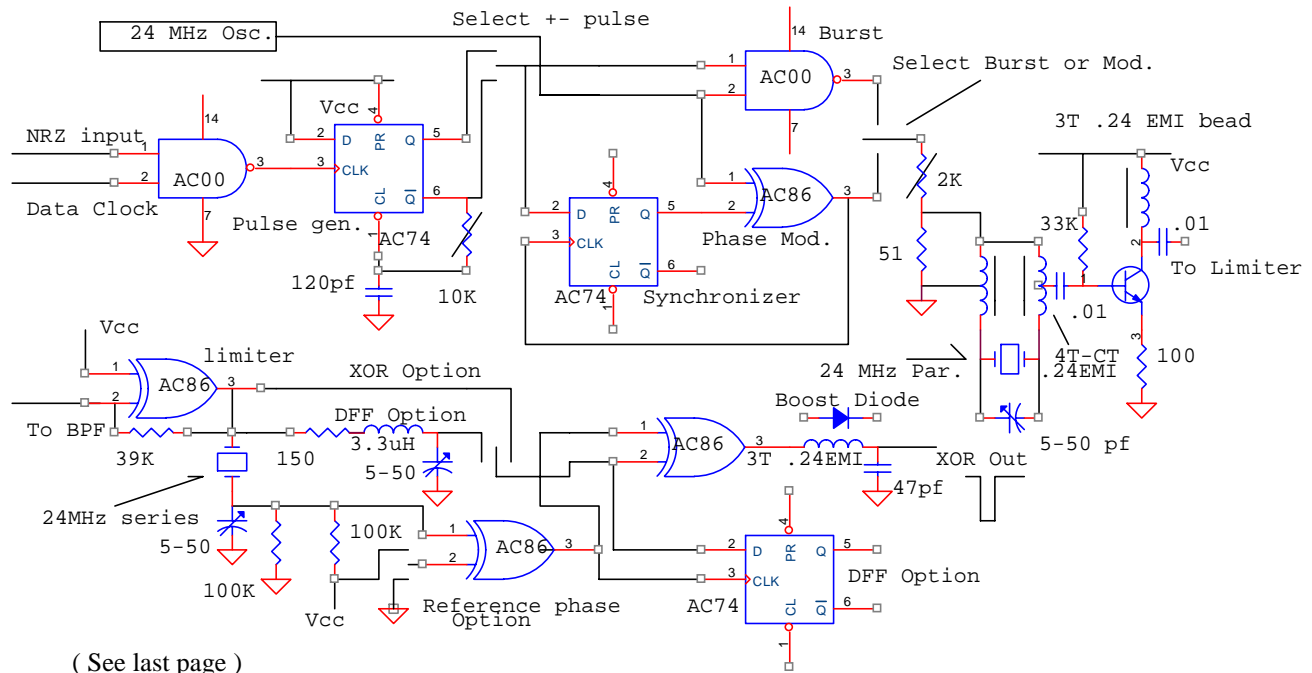


EXPERIMENTERS CIRCUIT



This circuit enables the experimenter to try Minimum Sideband Modulation with only 3 chips. (Also called Ultra Narrow Band Modulation, or modulation without sidebands).

The 24 MHz oscillator (about \$2.00 from Mouser or DigiKey) has a CMOS output to provide a carrier. U3 is a pulse generator that can have pulses as narrow as 1 RF cycle, or as wide as 20-30 cycles. Positive or negative pulses can be selected. Positive pulses yield a pulse string at the output of U1 (74AC00) for pulse testing of filters. Alternately, a negative pulse causes an RF stream with missing cycles. (Missing Cycle Modulation). The input AND gate and second Flip Flop synchronize the data with the RF cycles.

U2 (74AC86) is a phase reversing modulator that reverses phase with the pulse duration. This can be used for 3PRK modulation, or with wider variations WPRK or UWPRK. The output is selectable before the filter and attenuated to a level of -6 to -15 dBm.

The filter is a Walker bridge filter that has near zero group delay (near zero filter rise time). Ordinary filters cannot be used, they all have group delay.

The output of the filter has a narrow noise bandpass 2-3 kHz wide, with shoulders down 15dB +/- . Additional stages can be cascaded to get lower shoulders. This output is limited by U4 to drive a signal path and a reference path. See the paper on "FilterS" for more data on filters.

The signal path is through a very low Q phase shifter to drive either the optional FFlop or the XOR gate as phase detectors.

The reference path uses a series mode crystal to lock to the RF frequency at the phase with the longest ON time. It will reject any signal phase changes and yield a steady phase reference.

The phase detectors then have spiked outputs corresponding to the leading edge of the NRZ signal input. This can be used to obtain a data clock and restore the zeros and ones of the input signal. A pulse means a one, the absence of a pulse is a zero. For an XOR output, use no phase delay. For the DFF output, about 45 degrees is necessary.

The spectrum contains low level Fourier amplitude products, which are lowered by the filter. They do not have any effect on the detected phase angle as they are reduced or removed.

This method effectively transmits a signal that can be said to have no useful sidebands, since all the useful information is in the carrier. There are no BESSEL sidebands, even though the carrier has 180 degree abrupt change phase modulation.

The method is now in use on microwave links and will soon be tested on satellites. An Amateur transmitter and receiver have been built and tested. Meeting FCC specifications is easy with this hardware. It has no bandwidth, regardless of data rate. Data rates up to 3 Mb/s are possible using a 24 MHz IF.

Full details on Very Minimum Sideband Keying theory can be obtained from <VMSK.org >.

See also Microwaves and RF Magazine, Dec. 2003. Decoding and clock restoration circuits are available from www.VMSK.org.

Five US patents plus numerous foreign patents have been granted on this particular Ultra Narrow Band method. There are other (competing) methods patented or pending.(FK, XGt, UWDK,). This is the most effective method known to the author.

The bandpass filter inductors (transformers) shown are an EMI snubber bead used to remove parasites etc. They have a very low Q in the circuit and resemble an almost pure resistance. The inductor used was a Fair-Rite EMI bead, .239 with turns center tapped..(Mouser). The inductor in the phase shifter is a 3.3 uH coil --with Q- not an EMI bead. This coil need not be adjustable.

The filter crystals recommended are cylindricals, such as the Epson CSCS301-24..M-C, or ECS240-S-4, or Citizen CS10, CSA or CMR309.. CYLINDER type crystals are recommended, but the HC49 holder is acceptable in the series mode. Parallel crystals in an HC49 holder have undesirable spurs above the resonant frequency.

The transistor used was a Fairchild BF240. Almost any high frequency transistor can be used. On the Net -- go to <www.VMSK.org> for latest design details.

Adding a low pass filter (Example -pass 24 MHz, cutoff 48 for a 48 MHz IF) will clean up the waveform.. This low pass filter is added after the XOR phase detector.

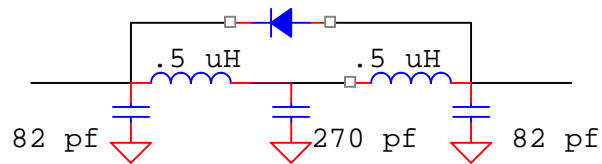


Fig. 2. Low pass filter and boost diode for 48 MHz. The boost diode reduces filter loss.

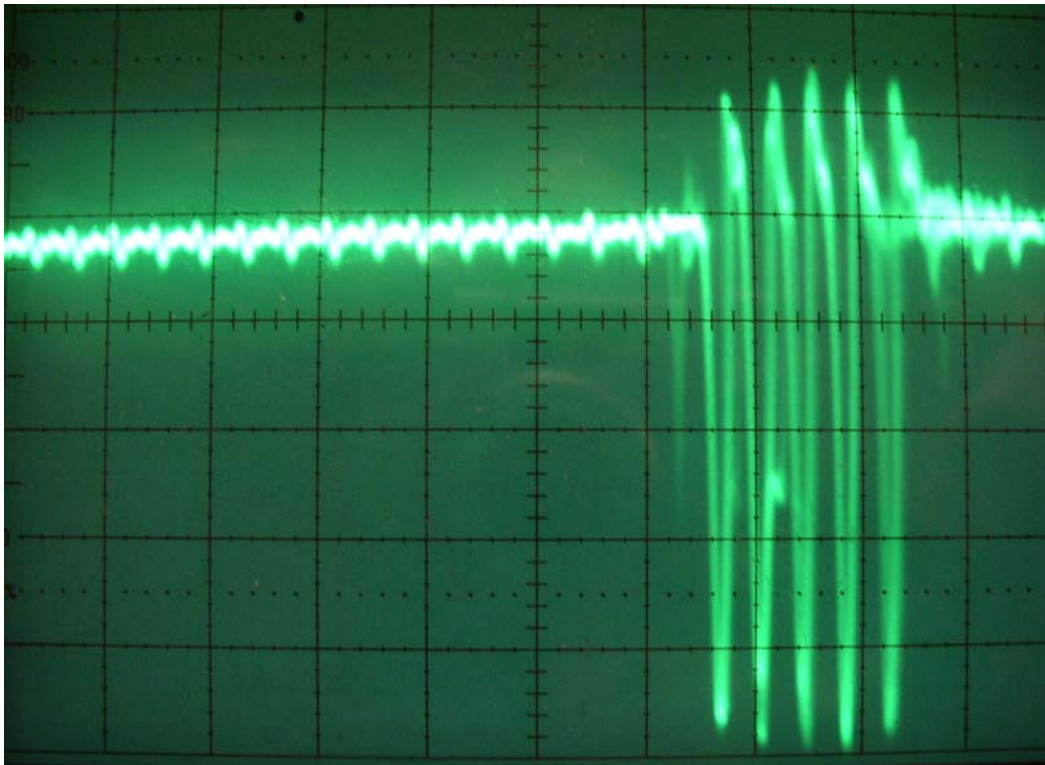


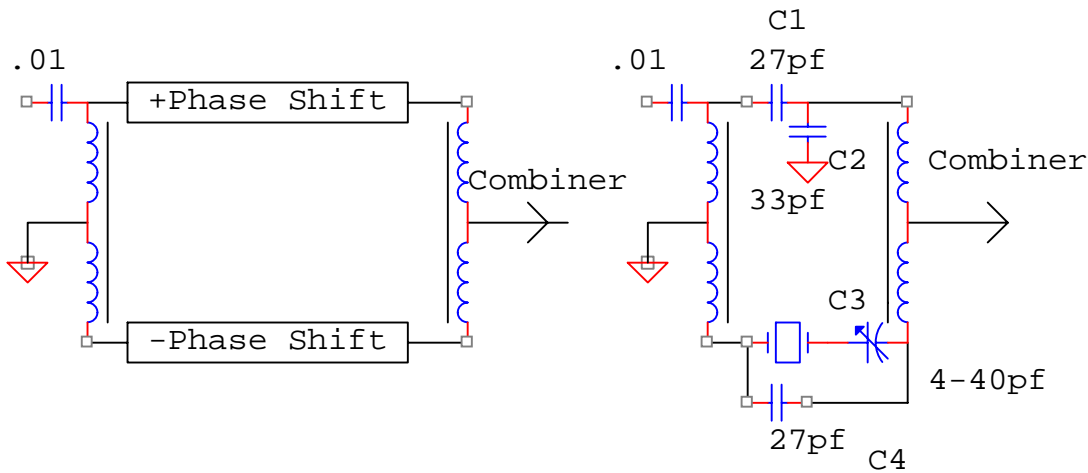
Fig. 3. Detected waveform after two stages of near zero group delay filtering. This is the XOR detector output with the waveform passed through the low pass filter of Fig. 2. The first down going spike to have enough level change to trigger the decoder will result in a detected digital one. There are no spikes for a digital zero.

This pattern is for the XOR modulator in Fig. 1, with 5 cycles out of a bit period reversed in phase, as set by the pulse width timing (approximately 1 volt per div.). This photo shows the filter had almost no group delay. (The rise time is approximately one IF cycle) and that a full 180 degree phase shift is being detected. 180 degrees is rail to rail with an XOR phase detector.(Vcc to 0).

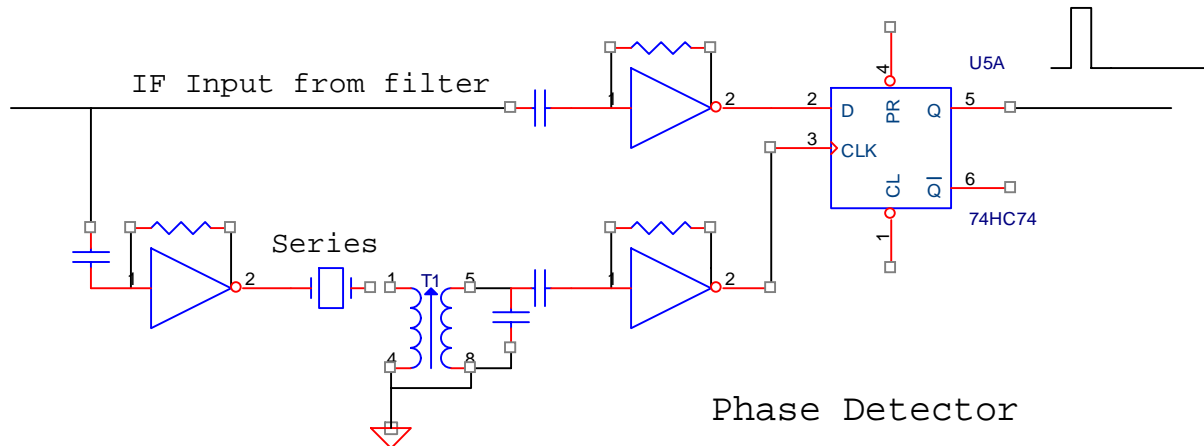
The narrow bandpass-zero group delay filter shown above is not the filter being used in practice. It passes low frequencies down to about 3-4 MHz and can give false results unless the conditions are understood. The bridge filter shown below is a much better filter for overall use.

The transformer is 4T center tapped on a FairRite .24 in. snubber bead. The trimmer caps are 1-40 pf Sprague. The load resistance is any value over 4.7K. The source resistance 47 Ohms.

Two capacitors C1 and C2 should be added to the filter, since they preserve more of the initial phase shift. They can be replaced by a single 1-40pf trimmer.



Missing cycle modulation (MCM or Holey) is not being used in practice, since it cannot be effectively limited and thus is usable only under controlled level conditions.



Instead of the circuit shown for data recovery, the use of the D flip flop alone is recommended. The XOR gate is not the best detector for this system in the presence of noise. This circuit eliminates many of the detector components shown in the original schematic. Figure 2 is not needed.